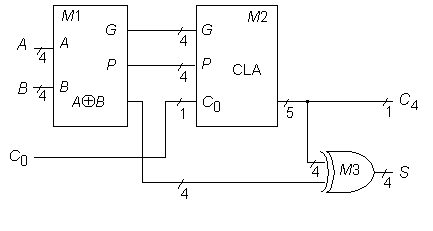
**74283 Fast Adder Circuit**



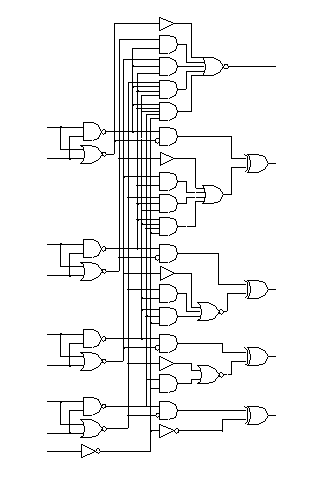
**Statistics:** 9 inputs; 5 outputs; 36 gates; [gate-level schematic](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74283gates.html)

**Function:** The 74283 fast adder can be modeled as shown above. The module [M1](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74283m1.html) produces the generate, propagate, and XOR functions. The module M2 is similar to the [74182](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74182.html). The XOR word gate M3 produces the sum function.

**Models:**

* [74283 ISCAS-85 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74283.isc)
* [74283 Verilog structural model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74283.v)
* [74283 behavioral model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74283b.v)
* [74283 complete gate-level tests (C0, A[3:0], B[3:0])](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74283.tests)

**74283 Gate-Level Schematic**



**74283 Module M1**

